Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-56. (Canceled)

57. (Previously Presented) A process for producing an electronic component, comprising the steps of:

providing (A) a laminate of a conductive inorganic material later, an insulating layer, and a conductive inorganic material layer, or (B) a laminate of a conductive inorganic material later and an insulating layer;

wet etching the conductive inorganic material layer in the laminate thereby patterning the conductive inorganic material layer;

laminating a dry film resist onto said laminate in which the conductive inorganic material layer has been patterned;

patterning the dry film resist, the dry film resist being developable with an aqueous solution and being able to be separated by the aqueous solution;

treating the thus patterned dry film resist with ultraviolet light irradiation and/or heat thereby improving the resistance of the dry film resist to the etchant for the insulating layer; and

wet etching the insulating layer through the patterned dry film resist by an aqueous basic solution.

58. (Original) The process for producing an electronic component according to claim 57, wherein the surface of the dry film resist has fine concaves and convexes.

59. (Original) The process for producing an electronic component according to claim 58, wherein the fine concaves and convexes are provided by embossing.

60. (Canceled)

61. (Canceled)

62. (Original) The process for producing an electronic component according to claim 57, wherein the insulating layer is patterned by the wet etching in such a manner that a dry film resist is laminated under reduced pressure onto the laminate in which the conductive inorganic material layer has been patterned, followed by wet etching of the laminate of the dry film resist.

63. (Previously Presented) The process for producing an electronic component according to claim 57, wherein the laminate of the dry film resist is wet etched by a method wherein, after the laminate of the dry film resist is exposed and developed to perform patterning, in order to improve the resistance of the dry film resist to the etchant for the insulating layer, treatment selected from ultraviolet light irradiation, heat treatment, and a combination of ultraviolet light irradiation with heat treatment is carried out.

64. (Original) The process for producing an electronic component according to claim 57, wherein the insulating layer in the laminate as the starting material has a thickness of 3 to 500 μm.

65. (Original) The process for producing an electronic component according to claim 57, wherein the thickness of the dry film resist is 1.1 to 5 times that of one conductive inorganic material layer in the laminate as the starting material.

66. (Original) The process for producing an electronic component according to claim 57, wherein the time necessary for wet etching of the insulating layer is not less than 10 sec and not more than 30 min.

67. (Original) The process for producing an electronic component according to claim 57, wherein the temperature in the wet etching of the insulating layer is not less than 10°C and not more than 120°C.

68. (Original) The process for producing an electronic component according to claim 57, wherein the single-layer structure or all the two or more insulation unit layers in the insulating layer are formed of an organic material.

69. (Original) The process for producing an electronic component according to claim 57, wherein the single-layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of a polyimide resin.

70. (Original) The process for producing an electronic component according to claim 57, wherein the single-layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of an inorganic material.

71. (Original) The process for producing an electronic component according to claim 57, wherein the single-layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of a composite composed of an organic material and an inorganic material.

72. (Original) The process for producing an electronic component according to claim 57, wherein the single-layer structure or all the two or more insulation unit layers in the insulating layer are formed of a polyimide resin.

73. (Original) The process for producing an electronic component according to claim 57, wherein the single-layer structure or at least one layer in the two or more insulation unit layers in the insulating layer is formed of a low-expansion polyimide having a coefficient of linear thermal expansion of not more than 30 ppm.

74. (Original) The process for producing an electronic component according to claim 73, wherein the insulating layer has a layer construction of adhesive polyimide – low-expansion polyimide – adhesive polyimide.

75. (Original) The process for producing an electronic component according to claim 74, wherein, in the insulating layer having a layer construction of adhesive polyimide –

low-expansion polyimide – adhesive polyimide, the two adhesive polyimides are different from each other in composition.

76. (Original) The process for producing an electronic component according to claim 57, wherein the etching liquid used for etching the insulating layer has a pH value of more than 9.

77. (Original) The process for producing an electronic component according to claim 57, wherein the single conductive inorganic material layer or both the two conductive inorganic material layers in the laminate are formed of copper or surface treated copper.

78. (Original) The process for producing an electronic component according to claim 57, wherein the single conductive inorganic material layer or both the two conductive inorganic material layers in the laminate are formed of copper alloy or surface treated copper alloy.

79. (Original) The process for producing an electronic component according to claim 57, wherein the single conductive inorganic material layer or both the two conductive inorganic material layers in the laminate are formed of stainless steel or surface treated stainless steel.

80. (Original) The process for producing an electronic component according to claim 57, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed of copper alloy or surface treated copper alloy.

81. (Original) The process for producing an electronic component according to claim 57, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed of copper or surface treated copper.

82. (Previously Presented) An electronic component produced by the process for producing an electronic component according to claim 57 .

83. (Previously Presented) A suspension for a hard disk drive, produced by the process for producing an electronic component according to claim 57.

84. (Previously Presented) A process for producing an electronic component, comprising the steps of:

providing (A) a laminate of a laminate of a conductive inorganic material layer, an insulating layer, and a conductive inorganic material layer, or (B) a laminate of a conductive inorganic material layer and an insulating layer;

wet etching the conductive inorganic material layer in the laminate, thereby patterning the conductive inorganic material layer;

laminating a dry film resist onto said laminate in which the conductive inorganic material layer has been patterned;

patterning the dry film resist, the dry film resist being developable with an aqueous solution and being able to be separated by the aqueous solution;

treating the thus patterned dry film resist with ultraviolet light irradiation and/or heat thereby improving the resistance of the dry film resist to the etchant for the insulating layer; and

wet etching the insulating layer through the patterned dry film resist by an aqueous basic solution, wherein

a thickness of the dry film resist is not less than 1.1 times that of one conductive inorganic material layer in the laminate, and

when the material to be etched is dipped in an etching liquid held at 70°C, a holding time of the dry film resist pattern is not less than one min.

85. (Original) The process for producing an electronic component according to claim 84, wherein at least one side of the dry film resist has fine concaves and convexes.

86. (Original) The process for producing an electronic component according to claim 85, wherein the fine concaves and convexes are formed by embossing.

87. (Canceled)

88. (Original) The process for producing an electronic component according to claim 84, wherein the insulating layer in the laminate is wet etched at a temperature of 10 to 120°C.

89. (Original) The process for producing an electronic component according to claim 84, wherein the etching liquid used for wet etching the insulating layer in the laminate has a pH value of more than 8.

90. (Original) The process for producing an electronic component according to claim 84, wherein the lamination of the dry film onto the laminate followed by wet etching is carried out by a method wherein, after the laminate of the dry film is exposed and developed to perform patterning, in order to improve the resistance of the dry film resist to the etchant for the insulating layer, treatment selected from ultraviolet light irradiation, heat treatment, and a combination of ultraviolet light irradiation with heat treatment is carried out.

91. (Original) The process for producing an electronic component according to claim 84, wherein the whole of one or more layers constituting the insulating layer in the laminate is formed of an organic material.

92. (Original) The process for producing an electronic component according to claim 84, wherein at least one layer constituting the insulating layer in the laminate is formed of a composite composed of an organic material and an inorganic material.

93. (Original) The process for producing an electronic component according to claim 84, wherein at least one layer constituting the insulating layer in the laminate is formed of a polyimide resin.

94. (Original) The process for producing an electronic component according to claim 84, wherein the whole of one or more layers constituting the insulating layer in the laminate is formed of a polyimide resin.

95. (Original) The process for producing an electronic component according to claim 84, wherein at least one layer constituting the insulating layer in the laminate is a low-expansion polyimide having a coefficient of linear expansion of not more than 30 ppm.

96. (Original) The process for producing an electronic component according to claim 84, wherein the insulating layer in the laminate has a layer construction of adhesive polyimide – low-expansion polyimide – adhesive polyimide.

97. (Original) The process for producing an electronic component according to claim 94, wherein, in the insulating layer having a layer construction of adhesive polyimide – low-expansion polyimide – adhesive polyimide, the two adhesive polyimides are different from each other in composition.

98. (Original) The process for producing an electronic component according to claim 84, wherein the whole of one or two conductive inorganic material layers in the laminate is formed of copper or surface treated copper.

99. (Original) The process for producing an electronic component according to claim 84, wherein the whole of one or two conductive inorganic material layers in the laminate is formed of copper alloy or surface treated copper alloy.

100. (Original) The process for producing an electronic component according to claim 84, wherein the whole of one or two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel.

101. (Original) The process for producing an electronic component according to claim 84, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed of copper alloy or surface treated copper alloy.

102. (Original) The process for producing an electronic component according to claim 84, wherein one of the two conductive inorganic material layers in the laminate is formed of stainless steel or surface treated stainless steel and the other is formed of copper or surface treated copper.

103. (Previously Presented) An electronic component produced by the process for producing an electronic component according to claim 84 .

104. (Previously Presented) A suspension for a hard disk drive, produced by the process for producing an electronic component according to claim 84 .